IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION

REDSTONE LOGICS LLC, Plaintiff, v. NXP USA, INC. Defendants.	Case No. 7:24-cv-00028-DC-DTG

PLAINTIFF'S SUR-REPLY CLAIM CONSTRUCTION BRIEF

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I. Introduction

Defendant's reply fails to address the shortcomings of their arguments noted in Plaintiff's response brief. Instead, Defendant misconstrues Plaintiff's arguments and outright ignores the clear disclosures of the patent.

II. Disputed Terms Requiring Construction

A. Term 1: "the first clock signal is independent from the second clock signal"

Defendant's reply fails to recognize the context of the disputed term. The clock signals that are claimed as independent from one another are the input signals to PLLs that provide output clock signals to a *set* of processor cores. *See* '339 at Cl. 1, 21. In this context, Defendant's reliance on Kim as showing disclaimer is misplaced.

Kim teaches a single clock source feeding a first PLL that in turn feeds further PLLs that each feed a single core. Dkt. 39-6 at [0024]. Kim does not teach grouping any of these single cores together. As such, there is no first and second clock signal that are inputs to PLLs that provide output clock signals to a set of processor cores. Defendant contends this is because any signal that is in any way derived from a single clock source cannot be independent from another such signal. But that conclusion is not supported by the prosecution history. All the applicant said was:

> In addition, the first clock signal is independent from the second clock signal. Instead, *Kim* discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores. See *Kim*, paragraphs [0024]-[0025] and FIGs 1 - 2.

Dkt. 39-9 at 10-11. Defendant ignores the applicant's reference to Kim's "apparatus comprising a multi-core processor" to focus exclusively on the reference to "a single clock source." *See* Dkt. 43 at 3-4. But looking at the apparatus of Kim, it becomes apparent there is no clear first or second

clock signal at all. With no set of processor cores, there is no clock signal as inputs to PLLs that provide output clock signals to a set of processor cores, as claimed:

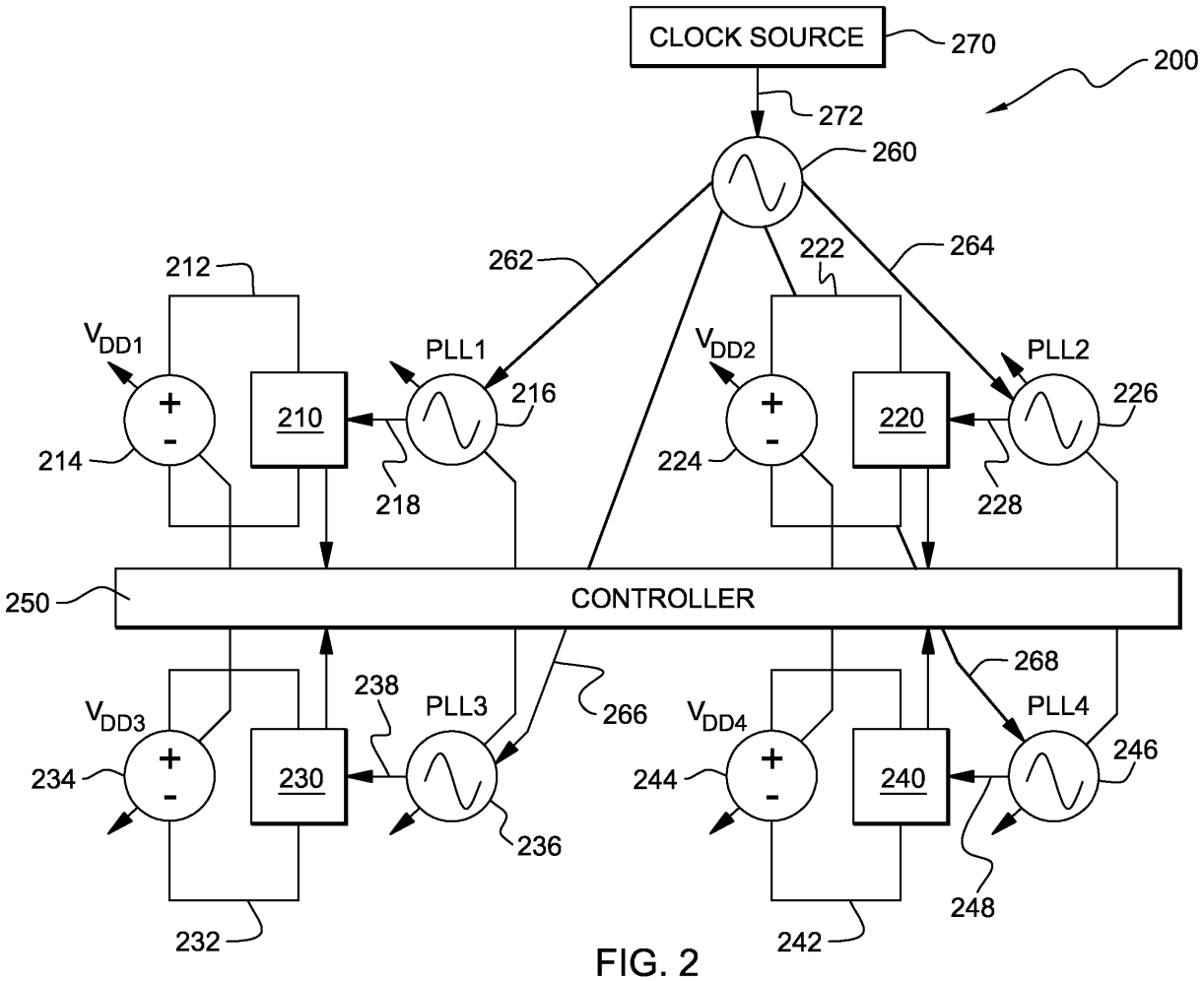


FIG. 2

Dkt. 39-9 at Fig. 2. For example, if Defendants are mapping all the cores of Kim to one of the claimed sets of cores, there could be a single clock signal as claimed but not a second clock signal that it could be independent from. And if Defendants are mapping two sets of two cores each (*e.g.*, 210 and 230 as the first set, and 220 and 240 as the second set), there could not be independent first and second clock signals as claimed, because there is only a single clock signal (272), not two

independent signals as claimed. At the very least, this demonstrates the applicant did not make a clear disavowal.

Defendant's citation to *Amgen* only further emphasizes that they are attempting to base disclaimer on a vague description of Kim. *Amgen* provides that a "***clear*** assertion [] whether or not actually required to secure allowance of the claim, may also create an estoppel." *Amgen Inc. v. Coherus BioSciences Inc.*, 931 F.3d 1154, 1159 (Fed. Cir. 2019). While there are multiple reasons Kim does not anticipate or render obvious any claim, there are multiple reasons why Kim's "apparatus comprising a multi-core processor [] having a single clock source" does not meet the "first clock signal is independent from the second clock signal." This is far from the "clear assertion" mandated by *Amgen*. The fact that the applicant "used 'independent' 11 times" when distinguishing Kim and Jacobowitz offers no further clarity.

Defendant's argument about the plain meaning of "independent" is similarly unavailing. Defendant's mathematical approach has no basis in either the art or in the intrinsic evidence and lacks even support from Defendant's own expert. What is in the intrinsic record is how the applicant used the term. In the examiner interview regarding Jacobowitz that resulted in amending the claim to include the disputed language, the applicant used "independent" interchangeably with "different." *See* Dkt. 39-8 at 2 ("clock signals 1 through 3 were different/independent clock signals…"). The applicant's own use of the term is more persuasive of its plain meaning than attorney argument.

Defendant's reply provides no basis to depart form the plain meaning of "independent" as "different."

B. Term 2: "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal"

Defendant pleads ignorance with no real intrinsic or extrinsic support, claiming "configured to receive" is so vague as to render the term indefinite. But Defendant's focus on "configured to" is merely a misplaced enablement argument. The reality is that "dynamically" is a routinely used term in the art to mean intentionally changing, rather than static, voltages and frequencies. A POSITA would readily understand not just how to send such a signal but also how to receive, i.e. a configuration, such a signal.

While Plaintiff will readily agree that "configured to dynamically receive" requires "configured," not just receipt of a dynamic signal, that does not mandate the specification teach every, or indeed any, way that can be done. Various configurations that enable sending and receiving dynamic signals in the multi-core processor field were known to a POSITA. The patent explains "dynamically adjusting the power profile for a stripe in response to changes in computational requirements may reduce power consumption for a multi-core processor, such adjustments may take some period of time to stabilize." '339 Patent at 3:16-20. It is that stabilization period that different configurations of both sending and receiving effect. As this is not the focus of the patent, it is left to the skill of a POSITA to provide their preferred configuration. A POSITA, understanding sending a dynamic signal, understands the corollary of receiving such a signal. Indeed, NXP's IPR expert[1] provides much the same, relying on a reference's teaching of "dynamically providing supply voltages and clock frequencies" also suggests the correlary of "dynamically receiv[ing] the same." Ex. 1 at ¶92. Further, one such configuration to dynamically

[1] While in contrast to MediaTek, NXP uses a different expert for claim construction than its IPR petition and thus does not suffer the inconsistency problem, NXP's IPR expert still provides opinions relevant as extrinsic evidence.

receive may be derived from Cheng as explained in Plaintiff's responsive brief, but other prior art may similarly provide configurations.

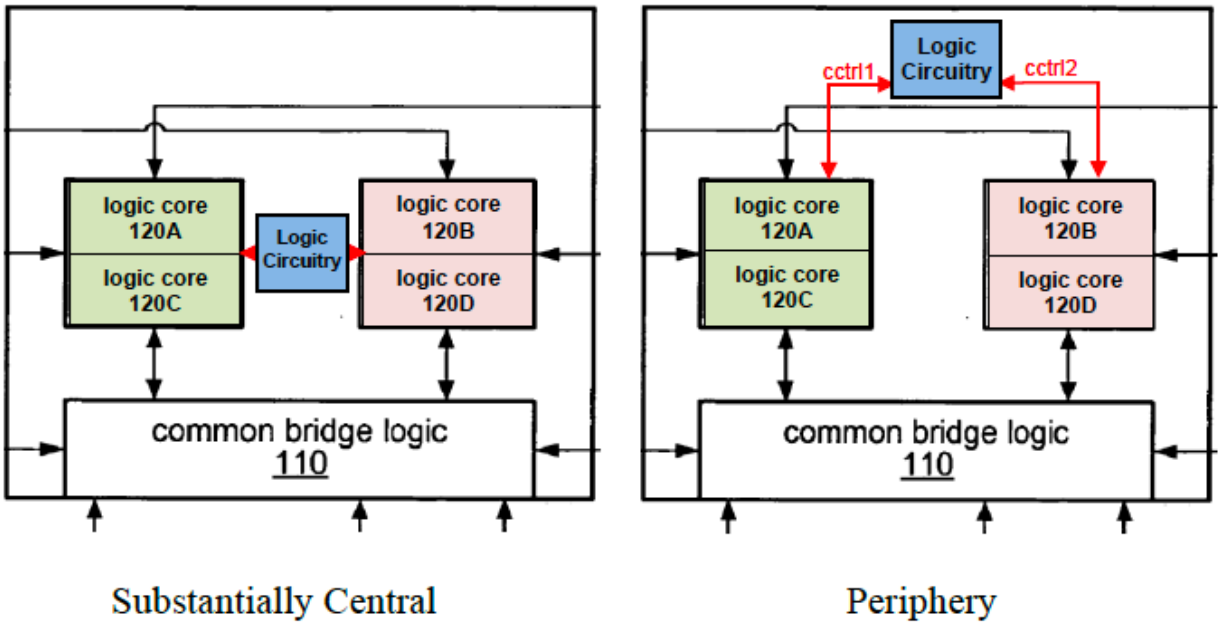
Defendant's complaints that Cheng was not incorporated into the specification itself or was only disclosed in an IDS after the claims were allowed are inapposite. The question of indefiniteness is "to be evaluated from the perspective of someone skilled in the relevant art." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 908, 134 S. Ct. 2120, 2128, 189 L. Ed. 2d 37 (2014); *see also Augme Techs., Inc. v. Yahoo! Inc.*, 755 F.3d 1326, 1340 (Fed. Cir. 2014) (rejecting indefiniteness argument that specification does not disclose the limitation as "based on the wrong legal standard, i.e., written description or enablement as opposed to indefiniteness."). Cheng demonstrates the knowledge of someone skilled in the art as of the priority date of the '339 Patent. Thus, Cheng's discussions of "dynamic voltage and frequency scaling (DVFS) for fine-grained chip multi-processors" is germane to how a POSITA would understand "configured to dynamically receive." Its disclosures for how a multi-core processor can be configured to both generates/sends and receives dynamic voltages and frequencies would have been known to a POSITA as just one example of being "configured to dynamically receive."

A POSITA would fully understand the scope and meaning of "configured to dynamically receive." Dynamic voltage and frequency are well-known techniques in the art as are both configurations to send and receive such signals. In this light, Defendant has no basis to suggest the configuration needed to receive such signals is not known to a POSITA.

C. Term 3: "located in a periphery of the multi-core processor"

Defendant's arguments misconstrue the standard for definiteness. The question is not if a Defendant can identify a particular situation where a limitation cannot be ascertained —though it has not. That is a question of application, not scope. Indeed, this situation is far from the "lone

example" in *Interval Licensing*. Indeed, if the scope was so undefinable, NXP's IPR expert would not have made the same distinction as made in Plaintiff's responsive brief that "periphery" refers to "along the perimeter of the multi-core processor" as opposed to centrally located. Ex. 1 at ¶¶105, 130.



If a POSITA can understand a term well enough to call a modification to meet the term an "obvious design choice," *Id.* at ¶105, that term is not indefinite. Here, a POSITA would readily understand the scope of "periphery" based on is plain meaning.

First, Defendant's reference to a distributed architecture of a multi-core processor is a red herring. Such a focus on what might infringe is a question of application, not scope. *See Spansion, Inc. v. Int'l Trade Comm'n*, 629 F.3d 1331, 1346 (Fed. Cir. 2010) ("Difficulty or complexity of the infringement analysis does not necessarily speak to whether a claim is definite or not."). That Dr. Villasenor's incomplete examples may not clearly demonstrate a multi-core processor with a periphery, is of no consequence. As noted in Plaintiff's response brief, Dr. Villasenor's "real-world" examples are too simplistic to effectively address the term. Adding the components needed

for a functioning multi-core processor clarifies any ambiguity Dr. Villasenor creates. *See* Dkt. 41 at 12-13. Defendant fails to address this in any meaningful way.

Second, unlike the "lone example" that "unobtrusive manner that does not distract a user" in *Interval Licensing*, Defendant does not credibly contend "periphery" is a term of degree. Again, "periphery" is not a term of degree, it is a relational term. Unlike "unobtrusive," "periphery" is not concerned with the opinion or attention span of a user. It refers instead to the edge of a space, here "the multi-core processor." The specification provides one example of what that might look like in Figure 1, but as noted with Dr. Villasenor's figures, a POSITA would readily understand the edge of a variety of other architectures.

Defendant has not met its burden to demonstrate "periphery of the multi-core processor" is indefinite. Indeed, Defendant has not even identified a single example of where a POSITA could not determine a periphery.

D. Term 4: "located in a common region that is substantially central to the first set of cores and second set of processor cores"

Recognizing that the disputed term is readily understood by a POSITA, Defendant turns to splitting hairs and arguing breadth results in indefiniteness. Neither meets Defendant's burden.

First, "common" does not render "common region" indefinite. Again, Defendant concedes a POSITA would understand "common region" as a region "shared by first and second sets of processor cores." *See* Dkt. No. 39 at 19. The *only* basis Defendant has for disregarding what it concedes a POSITA would understand is claim differentiation. *See id*. Even if as Defendant alleges without support, that its argument did not rely on claim differentiation, this reflects the plain meaning of "common" as used in the patent. *See* '339 at 2:37-40.

Second, Defendant's complaint that the clear standard disclosed in the Patent regarding "substantially central" is "overbroad" does not reflect the law. It is axiomatic that "breadth is not

indefiniteness." *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017). Defendant's contention that "'substantially central' remains indefinite with respect to numerous other real-world processor configuration," Dkt. 43 at 10, is unsubstantiated. Dr. Villasenor's discussion of distributed architectures is inapposite. These examples never address a multi-core processor with even the claimed components which are necessary to compose a "common region" let alone ascertain its location or existence.

The disclosures of Figure 1, in combination with the claim language itself, is sufficient to provide a POSITA a standard for measuring "substantially central." The specification provides for various locations of control blocks along the sides or "in a common area located near the center of the multi-core processor." '339 Patent at 2:31-40. While not definitional, this provides a standard for a POSITA to measure "substantially central." The claim language provides further guidance, placing the control blocks in a common region substantially central to the first and second set of processor cores. Defendant has no evidence that a POSITA would not find this portion of the specification provides sufficient guidance. Indeed, NXP's IPR expert appears to have followed this guidance, distinguishing "along the perimeter" from "substantially central. Ex. 1 at ¶105.

For these reasons, Defendant has not shown by clear and convincing evidence that Claim 14 is indefinite. Claim 14 should be given its plain and ordinary meaning.

III. Conclusion

For the reasons provided above, all disputed terms should be given their plain and ordinary meaning. Defendant has failed to meet its burden to show any term is indefinite.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I certify that on February 5, 2025, a true and correct copy of the foregoing document was electronically filed with the Court and served on all parties of record via the Court's CM/ECF system.

/s/ Reza Mirzaie
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